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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/678,175	09/28/2000	Victor Konrad	042390.P9573	2921

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EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/678,175	KONRAD ET AL.	
	Examiner	Art Unit	
	Helen B Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-19 and 22-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-19 and 22-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09/28/2000* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 09/678,175 filed 09/28/2000 and amendment filed 08/16/2004.

2. Claims 1-3, 6-19, 22-40 remain pending in the Application.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/16/2004 has been entered.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3, 6-19, 22-40 are rejected under 35 U.S.C. 102(e) as being unpatentable by Shau (US Patent 6,492,835).

With respect to claims 1, 10, 17, 24, 29 and 36 Shau teaches method, a program storage device readable by a machine comprising instructions by using CAD including

all attributes of computer programming performance (col. 4, ll.22-24; col. 5, ll.39-41), comprising determining an optimum (col. 4, ll.31-33) splitting variable for dividing a programmable logic array (PLA) into at least two sub-PLAs as shown on the Fig. 3(b), wherein 321-324 are partitions (sub-PLAs) (col. 8, ll.16-20; col. 12, ll.15-19), each sub-PLA of the at least two sub-PLAs having an AND plane and an OR plane as shown on the Figs. 3(b) and 3(a) each partition (321-324) has AND array (on the left side (161)) and OR array (on the right side (162)) as shown on the Fig. 1(f), a first sub-PLA of the at least two sub-PLAs includes products in which the splitting variable is in complemented form, a second sub-PLA of the at least two sub-PLAs includes products in which the splitting variable is in uncomplemented form, the splitting variable corresponding to a specific input, output and product in a set of equations representing the PLA by simplifying sub-PLAs by having used and unused input/output lines (splitting variables) as shown on the Fig. 3(b) first partition (321) has three unused input signals (Ie, Id, If) and the rest of them are used, which selectively might be removed for optimization and simplification (col. 8, ll.63-67; col. 9, ll.1-9); dividing a set of equations representing a PLA into a first set of equations representing the first sub-PLA and a second set of equations representing the second sub-PLA based on the splitting variable within dividing the equations describing the logic relationships between input signals and output signals in the AND array and OR array of the whole PLA into multiple sets of the equations according the partitions of the PLA (col. 5, ll.46-67; col. 8, l.61; col. 9, l.4; Fig. 2(a)); determining a topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA as shown on the Fig.

3(c) which reflects the simplified partitions (sub-PLAs) of the PLA according the equations describing the sub-PLAs after dividing the PLA into partitions (col. 9, ll.1-9); applying gating logic to the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA (col. 28-29); and controlling power consumption in the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA so only one of the topological circuit representation of the first sub-PLA and the second sub-PLA contributes to power consumption (col. 12, ll.26-28; ll.32-33), wherein an OR plane of the topological circuit representation of the first sub-PLA is interleaved with an OR plane of the topological circuit representation of the second sub-PLA as shown on the Fig. 3(c) wherein the OR plane (381) of the first sub-PLA (331) is interleaved with the OR plane (384) of the second sub-PLA (334).

With respect to claims 2, 11, 18, 25, 30 and 37 Shau teaches the PLA to be divided is partially optimized by computer aided design by using the PLA CAD tools and with the ability of CAD tools to break down complex logic calculations into series of single step logic operations such as synthesizing the design of integrated circuit (col. 1, ll.20-30; col. 12, ll.41-44).

With respect to claims 3, 19, 31 and 38 Shau teaches merging an output of the equations representing the first sub-PLA with an output of the equations representing the second sub-PLA, wherein merging the output of the equations representing the first sub-PLA with the equations representing the second sub-PLA forms a logical equivalent of the PLA as shown on the Fig. 3(c) and described by flowchart depicted on the Fig.

2(d) by connecting all sub-PLAs and equations describing each sub-PLA to construct the PLA (col. 8, ll.43-52; col. 9, ll.34-39).

With respect to claims 6, 22, 32 and 39 Shau teaches the equations representing the first sub-PLA includes a plurality of products where the splitting variable is complemented and the equations representing the second sub-PLA includes a plurality of products where the splitting variable is uncomplemented by simplifying sub-PLAs by having used and unused input/output lines (splitting variables) as shown on the Fig. 3(b) first partition (321) has three unused input signals (Ie, Id, If) and the rest of them are used, which selectively might be removed for optimization and simplification (col. 8, ll.63-67; col. 9, ll.1-9).

With respect to claims 7 and 33 Shau teaches delaying a clock to an OR plane of one of the topological circuit representation of the first sub-PLA and the topological circuit representation of the second sub-PLA as shown on the Fig. 3(d) wherein output circuits (330), which are connected to OR planes of the first sub-PLA and second sub-PLA and contain the latch (341) which is connected to the gate (col. 9, ll.40-49).

With respect to claims 8, 23, 34 and 40 Shau teaches determining the optimum splitting variable further comprises avoiding unbalanced columns in an AND plane of the set of equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the set of equations representing the PLA by performing the procedure of balancing the sizes of sub-PLAs within moving minterms which are the functions of the inputs (splitting variables), wherein the balancing of the sub-PLAs is one of the part of the optimization during the partitioning of the PLA (col.8, ll.12-17).

With respect to claims 9 and 35 Shau teaches determining a topological circuit representation of first sub-PLA and the second sub-PLA is created by computer aided design (col. 5, ll.41-43; col. 9, ll.31-33).

With respect to claims 12 and 26 Shau teaches the equations representing the plurality of sub-PLAs are divided recursively based on a determined optimum splitting variable for each equation representing a sub-PLA as shown on the Fig. 2(c) wherein the process of optimization is repeatedly done within repeatedly moving minterms across partitions to balance the sizes of sub-PLAs until optimum partition is done (col. 8, ll.16-17).

Wit respect to claims 13 and 14 Shau teaches each product of the equations representing the plurality of sub-PLAs is obtained by omitting literals in the equations representing the PLA by simplifying the sub-PLAs and the equations describing them by removing the unused input lines from the layout of the sub-PLA and their equations as shown on the Fig. 3(c) (col. 8, ll.63-67; col. 9, ll.1-2); a product of the omitted literals is used in the topological circuit representation of the plurality of sub-PLAs to gate a clock of each product of the plurality of sub-PLAs as shown on the Fig. 3(d) wherein output circuits (330), which are connected to OR planes of the first sub-PLA and second sub-PLA and contain the latch (341) which is connected to the gate (col. 9, ll.40-49).

With respect to claims 15, 16, 27 and 28 Shau teaches the step of determining the optimum splitting variable further comprises avoiding unbalanced columns in an AND plane of the equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the equations representing the PLA by performing the

procedure of balancing the sizes of sub-PLAs within moving minterms which are the functions of the inputs (splitting variables), wherein the balancing of the sub-PLAs is one of the part of the optimization during the partitioning of the PLA (col.8, ll.12-17).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

A. M. Thompson
Primary Examiner
Technology Center Z800